SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-179129; filed September 11, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a semiconductor device.

BACKGROUND

A plurality of semiconductor elements formed in a semiconductor wafer are divided into a plurality of semiconductor chips by dicing the semiconductor wafer along dicing regions provided in the semiconductor wafer. A leakage current may flow through an edge portion of the semiconductor chip formed by the dicing, and thereby the semiconductor chip may be broken down.

An example of related art includes JP-A-2009-177039.

DESCRIPTION OF THE DRAWINGS

FIGS. 1A and 1B are schematic views illustrating a semiconductor device according to a first embodiment.

FIG. 2 is a schematic sectional view illustrating a fabrication method of the semiconductor device according to the first embodiment.

FIG. 3 is a schematic sectional view illustrating the fabrication method of the semiconductor device according to the first embodiment.

FIG. 4 is a schematic sectional view illustrating the fabrication method of the semiconductor device according to the first embodiment.

FIG. 5 is a schematic sectional view illustrating the fabrication method of the semiconductor device according to the first embodiment.

FIG. 6 is a schematic sectional view illustrating the fabrication method of the semiconductor device according to the first embodiment.

FIG. 7 is a schematic sectional view illustrating the fabrication method of the semiconductor device according to the first embodiment.

FIG. 8 is a schematic sectional view illustrating the fabrication method of the semiconductor device according to the first embodiment.

FIG. 9 is a schematic sectional view illustrating the fabrication method of the semiconductor device according to the first embodiment.

FIG. 10 is a schematic sectional view illustrating the fabrication method of the semiconductor device according to the first embodiment.

FIGS. 11A and 11B are a schematic view and a schematic diagram illustrating a semiconductor device according to a second embodiment.

DETAILED DESCRIPTION

[0004]Exemplary embodiments provide a semiconductor device which prevents a leakage current from flowing through an edge portion of a semiconductor chip.

[0005]In general, according to one embodiment, a semiconductor device includes a p-type semiconductor substrate which includes a first surface, a second surface, and an end portion, and includes an n-type region that is provided in a corner portion between the first surface and the end surface; a nitride semiconductor layer which is provided on the first surface; and an electrode which is provided on the nitride semiconductor layer.

[0007]Embodiments of the invention will be hereinafter descried with reference to the drawings. In the following description, the same symbols or reference numerals will be attached to the same or similar members or the like, and description of the members or the like described once will be appropriately omitted.

[0008]In addition, in the specification, a “GaN-based semiconductor” is a general term for a semiconductor that contains gallium nitride (GaN), aluminum nitride (AlN), indium nitride (InN), and an intermediate composition of those.

First Embodiment

[0009]A semiconductor device according to the present embodiment includes a p-type semiconductor substrate which includes a first surface, a second surface, an end surface, and an n region provided in a corner portion between the first surface and the end surface, a nitride semiconductor layer which is provided on the first surface, and an electrode which is provided on the nitride semiconductor layer.

[0010]FIGS. 1A and 1B are schematic views illustrating a semiconductor device according to the present embodiment. FIG. 1A is a sectional view of the semiconductor device, and FIG. 1B is a top view of the semiconductor device.

[0011]The semiconductor device according to the present embodiment is a semiconductor chip 100. The semiconductor chip 100 includes a p-type silicon substrate (p-type semiconductor substrate) 10, a GaN-based semiconductor layer (nitride semiconductor layer) 12, a source electrode 14, a drain electrode 16, and a gate electrode 18. The p-type silicon substrate 10 includes a p-type region 10a and an n-type region 20. The GaN-based semiconductor layer 12 includes a first GaN-based semiconductor film 12a and a second GaN-based semiconductor film 12b.

[0012]A semiconductor element is formed in the semiconductor chip 100. The semiconductor element is, for example, a high electron mobility transistor (HEMT).

[0013]The p-type silicon substrate 10 includes a first surface P1, a second surface P2, and an end surface E. The p-type silicon substrate 10 contains p-type impurity. The p-type impurity is, for example, boron (The output terminal a). The p-type impurity concentration of the p-type silicon substrate 10 is, for example, higher than or equal to 1´1014 cm-3 and lower than or equal to 5´1018 cm-3. In addition, the p-type impurity concentration of the p-type silicon substrate 10 is, for example, higher than or equal to 1´1014 cm-3 and lower than or equal to 5´1015 cm-3.

[0014]The p-type silicon substrate 10 includes the n-type region 20 in a corner portion between the first surface P1 and the end surface E. The n-type region 20 contains n-type impurity. The n-type impurity is, for example, phosphorus (P) or arsenic (As). The n-type impurity concentration of the n-type region 20 is higher than the p-type impurity concentration of the p-type silicon substrate 10. The n-type impurity concentration of the n-type region 20 is, for example, higher than or equal to 1´1018 cm-3 and lower than or equal to 1´1021 cm-3.

[0015]The p-type impurity concentration of the p-type silicon substrate 10, and the n-type impurity concentration of the n-type region 20 can be measured by a secondary ion mass spectrometry (SIMS).

[0016]The n-type region 20 is formed in the p-type silicon substrate 10, and thereby a PIN diode is formed in the p-type silicon substrate 10. The p-type region 10a of the p-type silicon substrate 10 becomes an anode electrode of the PIN diode, and the n-type region 20 becomes a cathode electrode of the PIN diode.

[0017]As illustrated in FIG. 1B, the n-type region 20 is provided to surround the p-type region 10a, in the first surface P1. The p-type region 10a is a part of the p-type silicon substrate 10, and a part thereof becomes a region with p-type conductivity in contact with the first surface.

[0018]Bonding between the n-type region 20 and the p-type region 10a is terminated at the end surface E of the p-type silicon substrate 10.

[0019]The GaN-based semiconductor layer 12 has a stacking structure in which the second GaN-based semiconductor film 12b is stacked on the first GaN-based semiconductor film 12a. The second GaN-based semiconductor film 12b is provided on the first GaN-based semiconductor film 12a. The bandgap energy of the second GaN-based semiconductor film 12b is greater than the bandgap energy of the first GaN-based semiconductor film 12a.

[0020]The first GaN-based semiconductor film 12a is, for example, a gallium nitride (GaN) film. The second GaN-based semiconductor film 12b is, for example, aluminum gallium nitride (AlGaN).

[0021]The source electrode 14 of a HEMT, the drain electrode 16, and the gate electrode 18 are provided on a surface of the second GaN-based semiconductor film 12b. The source electrode 14, the drain electrode 16, and the gate electrode 18 are, for example, metals.

[0022]For example, a protection film which is not illustrated is provided on the source electrode 14, the drain electrode 16, and the gate electrode 18. The protection film is, for example, a silicon oxide film. It doesn’t matter if a gate insulating film which is not illustrated is provided between the second GaN-based semiconductor film 12b and the gate electrode 18.

[0023]A width (W1 of FIG. 1B) of the p-type silicon substrate 10 is greater than a width (W2 of FIG. 1B) of the GaN-based semiconductor layer 12. In other words, a part of the p-type silicon substrate 10 protrudes with respect to the GaN-based semiconductor layer 12, in an end portion of the semiconductor chip 100.

[0024]A part of the GaN-based semiconductor layer 12 is provided on the n-type region 20. An end portion of the GaN-based semiconductor layer 12 is provided on the n-type region 20. In other words, the end portion of the GaN-based semiconductor layer 12 and the n-type region 20 overlap each other on the first surface P1.

[0025]FIG. 2 to FIG. 10 are schematic sectional views illustrating a fabrication method of a semiconductor device according to the present embodiment.

[0026]First, a semiconductor wafer in which the GaN-based semiconductor layer 12 is provided on the p-type silicon substrate 10 is prepared (FIG. 2). The p-type silicon substrate 10 includes the first surface P1 and the second surface P2.

[0027]A thickness of the p-type silicon substrate 10 is, for example, greater than or equal to 1 mm and smaller than or equal to 2 mm. A thickness of the GaN-based semiconductor layer 12 is, for example, greater than or equal to 5 mm and smaller than or equal to 10 mm.

[0028]The GaN-based semiconductor layer 12 is provided on the first surface P1 of the p-type silicon substrate 10. The GaN-based semiconductor layer 12 is formed on the p-type silicon substrate 10 using an epitaxial growth method. The GaN-based semiconductor layer 12 includes, for example, a stacking structure of a GaN film and an AlGaN film. Two-dimensional electron gas (2DEG) which is formed on a boundary between the GaN film and the AlGaN film becomes a carrier of the HEMT.

[0029]Subsequently, a plurality of semiconductor elements are formed on the GaN-based semiconductor layer 12. The semiconductor element is the HEMT. For example, the source electrode 14 of the HEMT, the drain electrode 16, and the gate electrode 18 are formed on the surface of the GaN-based semiconductor layer 12 (FIG. 3). A protection film which is not illustrated is formed on the source electrode 14, the drain electrode 16, and the gate electrode 18. The protection film is, for example, a silicon oxide film.

[0030]Subsequently, the GaN-based semiconductor layer 12 of a dicing region is selectively etched until the p-type silicon substrate 10 is exposed (FIG. 4). The dicing region is a plan region with a predetermined width for dividing the plurality of semiconductor elements into a plurality of semiconductor chips by dicing. The dicing region is provided on the surface side of the GaN-based semiconductor layer 12. A pattern of the semiconductor element is not formed on the dicing region. For example, the dicing region is provided in a lattice shape on the surface side of the GaN-based semiconductor layer 12, such that the semiconductor elements are partitioned.

[0031]Etching of the GaN-based semiconductor layer 12 is performed by, for example, reactive ion etching (RIE). The etching of the GaN-based semiconductor layer 12 is performed by using, for example, a resist which is not illustrated, as a mask. The etching of the GaN-based semiconductor layer 12 may be performed by other etching, such as dry etching or wet etching.

[0032]Subsequently, n-type impurity is injected into the p-type silicon substrate 10 which is exposed in the dicing region using an ion injection method (FIG. 5). The n-type region 20 is formed by injecting n-type impurity using an ion injection method. The n-type impurity is, for example, phosphorus (P). The n-type impurity may be arsenic (As). The n-type impurity can be activated by, for example, laser annealing.

[0033]Subsequently, a supporting member 24 is bonded on the GaN-based semiconductor layer 12 (FIG. 6). The supporting member 24 adheres to the GaN-based semiconductor layer 12 using, for example, an adhesion layer 26.

[0034]The supporting member 24 has a function of reinforcing the semiconductor wafer, when the wafer is ground to be thinned. The supporting member 24 is, for example, a glass substrate.

[0035]Subsequently, the p-type silicon substrate 10 is ground to be thinned from the second surface P2 side of the p-type silicon substrate 10 (FIG. 7). The p-type silicon substrate 10 is thinned to have a thickness, for example, greater than or equal to 100 mm and smaller than or equal to 200 mm.

[0036]The thinning of the p-type silicon substrate 10 is performed by so-called back grinding. The thinning of the p-type silicon substrate 10 is performed by grinding using, for example, a diamond wheel.

[0037]Subsequently, a resin sheet 32 is attached to the second surface P2 side of the p-type silicon substrate 10 (FIG. 8). The resin sheet 32 is, for example, a dicing tape. For example, the resin sheet 32 is fixed to a metal frame for handling.

[0038]Subsequently, the supporting member 24 is peeled from the semiconductor wafer (FIG. 9).

[0039]Subsequently, regions of the p-type silicon substrate 10 between the GaN-based semiconductor layers 12 are cut by dicing with a blade from the first surface P1 side (FIG. 10). The p-type silicon substrate 10 is cut along the dicing regions.

[0040]Thereafter, the resin sheet 32 is peeled from the p-type silicon substrate 10, and thereby a plurality of semiconductor chips (semiconductor devices) 100 which are divided are obtained.

[0041]By the aforementioned fabrication method, the semiconductor chip 100 according to the present embodiment illustrated in FIG. 1 is easily fabricated.

[0042]Thereafter, each semiconductor chip 100 is embedded in a semiconductor package. For example, the semiconductor chip 100 is attached on a lead frame and sealed with a molding resin.

[0043]Hereinafter, actions and effects of the semiconductor device according to the present embodiment will be described.

[0044]A leakage current flowing through an end portion of the semiconductor chip may break the semiconductor chip. The breakdown of the semiconductor chip is made by, for example, a short circuit of an electrode formed on an upper surface of the semiconductor chip and the semiconductor substrate.

[0045]In the HEMT according to the present embodiment, a leakage current flows between, for example, the drain electrode 16 to which a high positive voltage is applied, and, for example, the p-type silicon substrate 10 which is fixed to a ground potential, and thereby heat is generated and insulation breakdown of an insulating film is made.

[0046]The leakage current flows into a surface of the end portion of the semiconductor chip 100 through moisture or conductive particles existing on a surface of the end portion of the GaN-based semiconductor layer 12 or the end surface E of the p-type silicon substrate 10. Alternatively, the leakage current flows into the end portion of the semiconductor chip 100 through a cracked portion which is formed in the end portion of the GaN-based semiconductor layer 12 at the time of dicing. Since a GaN-based semiconductor is harder and brittler than silicon, the GaN-based semiconductor is cracked easily more than silicon at the time of dicing. In addition, particularly, the GaN-based semiconductor formed on the silicon substrate is easily cracked by a stress difference therebetween.

[0047]In the present embodiment, the n-type region 20 is formed on the corner portion of the p-type silicon substrate 10, and thereby the PIN diode is provided. Even if a high positive voltage applied to the drain electrode 16 is applied to the corner portion of the end portion of the p-type silicon substrate 10 through the end portion of the GaN-based semiconductor layer 12, the PIN diode is reversely biased.

[0048]Hence, it is possible to prevent a leakage current from flowing between the drain electrode 16 and the p-type silicon substrate 10. Thus, the semiconductor chip 100 is prevented from being broken.

[0049]In addition, it is preferable that the end portion of the GaN-based semiconductor layer 12 and the n-type region 20 overlap each other on the first surface P1. Since the end portion of the GaN-based semiconductor layer 12 and the n-type region 20 overlap each other, it is possible to effectively prevent a leakage current from flowing through a cracked portion which is formed in the end portion of the GaN-based semiconductor layer 12.

[0050]In addition, in the present embodiment, the GaN-based semiconductor layer 12 comes into direct contact with the p-type region 10a of the p-type silicon substrate 10. For example, if the p-type silicon substrate 10 is fixed to the ground potential, a diode formed in a substrate portion behaves as a protection element and a breakdown voltage of the HEMT which is formed in the GaN-based semiconductor layer 12 increases, by the GaN-based semiconductor layer 12 and the p-type region 10a which are in contact.

[0051]As such, according to the semiconductor chip 100 according to the present embodiment, it is possible to prevent a leakage current from flowing through the end portion of the semiconductor chip 100. Thus, the semiconductor chip 100 is prevented from being broken, and the semiconductor chip 100 with increased reliability is realized.

Second Embodiment

[0052]A semiconductor device according to the present embodiment is different from the semiconductor device according to the first embodiment in that the semiconductor device according to the present embodiment further includes a first wire which electrically connects a source electrode to a p-type semiconductor substrate, and a second wire which electrically connects a drain electrode to an n-type region. Description of the content which overlaps that of the first embodiment will be omitted.

[0053]FIGS. 11A and 11B are a schematic view and a schematic diagram illustrating a semiconductor device according to the present embodiment. FIG. 11A is a sectional view of the semiconductor device, and FIG. 11B is an equivalent circuit of the semiconductor device.

[0054]The semiconductor device according to the present embodiment is a semiconductor package 200 in which a semiconductor chip is embedded. The semiconductor package 200 includes the p-type silicon substrate 10, the GaN-based semiconductor layer (nitride semiconductor layer) 12, the source electrode 14, the drain electrode 16, the gate electrode 18, a lead frame (metal layer) 40, a metal electrode 42, a first wire 44, and a second wire 46. The p-type silicon substrate 10 includes the p-type region 10a and the n-type region 20. The GaN-based semiconductor layer 12 includes the first GaN-based semiconductor film 12a, and the second GaN-based semiconductor film 12b.

[0055]A semiconductor element is formed in the semiconductor chip in the semiconductor package 200. The semiconductor element is, for example, a HEMT. The semiconductor chip is sealed with, for example, a molding resin which is not illustrated.

[0056]The p-type silicon substrate 10 adheres to the lead frame 40 of a metal by using an adhesion layer which is not illustrated. The adhesion layer is, for example, a solder or a conductive paste.

[0057]The metal electrode 42 is provided on the n-type region 20. It is preferable that the metal electrode 42 comes into Ohmic contact with the n-type region 20.

[0058]The first wire 44 connects the source electrode 14 to the lead frame 40. The first wire 44 is, for example, a boding wire of gold. The source electrode 14 and the p-type silicon substrate 10 are electrically to each other by the first wire 44.

[0059]The second wire 46 connects the drain electrode 16 to the metal electrode 42. The second wire 46 is, for example, a boding wire of gold. The drain electrode 16 and the n-type region 20 are electrically to each other by the second wire 46.

[0060]In the semiconductor package 200, a HEMT is connected in parallel with a PIN diode, as illustrated in FIG. 11B. The p-type region 10a of the PIN diode is connected to the source electrode 14 of the HEMT. The n-type region 20 of the PIN diode is connected to the drain electrode 16 of the HEMT.

[0061]For example, if a large surge current flows into the drain electrode 16 of the HEMT, a gate insulating film or the like may be broken down. According to the semiconductor module 200 according to the present embodiment, even if a large surge current flows into the drain electrode 16, it is possible to make the current escape into the source electrode 14 through the PIN diode by appropriately setting a breakdown voltage of the PIN diode. Thus, the semiconductor package 200 can be prevented from being broken.

[0062]According to the semiconductor package 200 according to the present embodiment, a leakage current does not flow through the end portion of the semiconductor package 200 by the same actions as in the first embodiment. Thus, the semiconductor package 200 is prevented from being broken, and the semiconductor package 200 with increased reliability is realized.

[0063]Furthermore, by providing a configuration in which the HEMT is connected in parallel with the PIN diode, the semiconductor package 200 is prevented from being broken due to a surge current. Thus, it is possible to realize the semiconductor package 200 in which reliability is more increased.

[0064]In the first and second embodiments, an example in which a semiconductor element is a HEMT is used, but the semiconductor element is not limited to the HEMT. Other semiconductor elements such as a horizontal diode can also be applied.

[0065]In addition, in the first and second embodiments, an example in which a silicon substrate is used for the substrate is used, but a semiconductor substrate other than a silicon substrate, for example, other substrates such as a silicon carbide (SiC) substrate can be applied.

[0066]While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a p-type semiconductor substrate which includes a first surface, a second surface, and an end portion, and includes an n-type region that is provided in a corner portion between the first surface and the end surface;

a nitride semiconductor layer which is provided on the first surface; and

an electrode which is provided on the nitride semiconductor layer.

2. The device according to Claim 1, wherein a width of the p-type semiconductor substrate is greater than a width of the nitride semiconductor layer.

3. The device according to Claim 1 or 2, further comprising:

a source electrode and a gate electrode which are provided on the nitride semiconductor layer,

wherein the electrode is a drain electrode, and

wherein the nitride semiconductor layer includes a first GaN-based semiconductor film, and a second GaN-based semiconductor film which is provided on the first GaN-based semiconductor film and whose bandgap energy is greater than bandgap energy of the first GaN-based semiconductor film.

4. The device according to any one of Claims 1 to 3, wherein n-type impurity concentration of the n-type region is higher than p-type impurity concentration of the p-type semiconductor substrate.

5. The device according to any one of Claims 1 to 3, wherein p-type impurity concentration of the p-type semiconductor substrate is higher than or equal to 1´1014 cm-3 and lower than or equal to 5´1015 cm-3.

6. The device according to any one of Claims 1 to 5, wherein a part of the nitride semiconductor layer is provided on the n-type region.

7. The device according to Claim 3, further comprising:

a first wire which electrically connects the source electrode to the p-type semiconductor substrate; and

a second wire which electrically connects the drain electrode to the n-type region.

8. The device according to any one of Claims 1 to 7, wherein the p-type semiconductor substrate is a p-type silicon substrate.

ABSTRACT

According to one embodiment, a semiconductor device includes a p-type semiconductor substrate which includes a first surface, a second surface, and an end portion, and includes an n-type region that is provided in a corner portion between the first surface and the end surface; a nitride semiconductor layer which is provided on the first surface; and an electrode which is provided on the nitride semiconductor layer.